ABSTRACT

A rectangular parallelepiped p-channel MOS transistor 21 having a height of H_B and a width of W_B is formed on a silicon substrate, and a gate oxide film is formed on a part of the top surface and the side surface of the p-channel MOS transistor 21. A source and a drain are formed on both sides of a gate electrode 26 to form a MOS transistor. A differential amplification circuit including MOS transistors 61 and 62 configures a limiter circuit. Thus, the gain of the limiter circuit can be designed large.